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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/17/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/835,021	Applicant(s) FELDMAN, ARNOLD R.	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign not mentioned in the description: Fig. 10 shows a dashed box "1010" that is not identified within the description. A proposed drawing correction, corrected drawing, or amendment to the specification to add the reference sign in the description, is required in reply to the Office action to avoid abandonment of the application.

The drawings are also objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "M1" and "M2" have been used to designate both an input pair of transistors within Fig. 1 and a current mirror type configuration in Fig. 4. Also, Fig. 3 shows capacitor "C1" coupled in parallel with inductor L1 to form a tank circuit in Fig. 3, but as an input capacitor in Fig. 4.

The drawings are objected to because "proportional" in each of blocks 820-850 of Fig. 8 should be --proportional--.

A proposed drawing correction or corrected drawings are required in reply to these last two sections of drawing objections within the Office Action to avoid abandonment of the application.

The objections to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 5, line 29 "385" should be --380--. Page 9: line 8 "455" should be --445--; line 20 "610 and is" is

believed to mean --610 is--; line 21 "axis 640" should be --axis 614--; and line 31 "644" should be --624--. The co-pending data on page 13, line 16 should be completed to ensure the correct information is available, and can be located/reviewed by the examiner. Appropriate corrections are required.

Claim Objections

Claims 7-15 are objected to because of the following informalities: Claim 7, line 6 should identify "second node" as --second output node-- for consistent labeling throughout the claims, thus minimizing possible confusion. Claim 12, line 1 "third and fourth switch" should be either --the third switch and the fourth switch-- or --the third and fourth switches-- since they had been previously described. Dependent claims 8-15 carry over the objection from claim 7. Appropriate corrections are required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1-6, and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear how "an input signal" on line 2 of claim 1 relates to "an RF signal" recited on line 1. If the same signal had been meant, then consistent labeling would minimize confusion. Similarly, how does "an input signal" in claim 8, lines 2-3 relate to "RF signals" recited in claim 7, line 1? Dependent claims 2-7 and 9-10 carry over the rejection from their respective independent claim.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hoover. Fig. 2 of Hoover shows a circuit comprising a well-known H-bridge (or full-bridge) circuit that closely corresponds to the applicant's Fig. 3 RF buffer amplifier. For example, Hoover's transistors P21,P22,N21,N22, first supply node +V, first output node 56, second output node 60, second supply node (ground), inductor L2, and capacitor C2 respectively correspond to the applicant's switches S1-S4, first supply node 360, first output node 390, second output node 380, second supply node 370, inductor L1, and capacitor C1. Therefore, a more detailed description of the structure is not necessary to one of ordinary skill in the art with respect to the applicant's claimed circuit. In operation, first/ fourth switches P21/N22 of Hoover's circuit are closed when second/third switches N21/P22 are open, and vice versa. The opening and closing of the switches depends upon the polarity of input signal IN. Since Hoover discloses frequencies up to 10 MHz (see column 3, lines 13-14), the circuit in Fig. 2 is also related to RF signals. Also, P21 and P22 are PMOS devices, wherein N21 and N22 are NMOS devices. Therefore, claims 7-11 and 13 are anticipated. As one of ordinary skill in the art would know, when P21 and N22 are conducting, a current will flow from +V to ground through P21,L2/C2,N22. When P21 and N22 are not conducting, no current will flow through

that path. P22 and N21 operate in a similar manner, except they conduct when P21,N22 are off. The currents through N21 and P21 are deemed first and fourth currents, respectively applied to a first terminal 86 of inductor L2, wherein the currents through N22 and P22 are deemed second and third currents, respectively applied to a second terminal 88 of inductor L2. Therefore, claims 1, 4 and 5 are anticipated. One of ordinary skill in the art would recognize L2 and C2 as a tank circuit, and since Hoover discloses the "parallel resonant circuits are tuned to the input signal frequency" (see column 3, lines 67-68), claims 2-3 are anticipated. One of ordinary skill in the art would know the current through their respective transistor would be geometrically proportional to the input signal, thus anticipating claim 6. For example, as a signal increases at node 50, the current through P21 would decrease, while the current through N21 would increase.

Claims 1-11, 13, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara. Gabara shows a circuit in Fig. 2A related to RF signals (see column 3, lines 2-5). The circuit comprises first device 30p coupled between first supply node Vdd and first output node C, and having a control electrode coupled to a first input node receiving input signal Vpch; second device 32p coupled between first supply node Vdd and second output node D, and having a control electrode coupled to a second input node receiving input signal Vpch; third device 30n coupled between first output node C and second supply node Vss, and having a control electrode coupled to second output node D; fourth device 32n coupled between second output node D and second supply node Vss, and having a control electrode coupled to first output node C; and an inductor 25

coupled between output nodes C and D, anticipating claim 16. The first-fourth devices can also be deemed first-fourth switches. Although Fig. 2A shows input signal Vpch at the gates of both 30p and 32p, one of ordinary skill in the art would recognize them as being complementary signals. Otherwise, if both transistors are on, nodes C and D would both be pulled up to Vdd. Therefore, when the input signal to the gate of first switch 30p goes low (and the input signal to the gate of second switch 32p goes high to turn the second switch off), first switch 30p begins to conduct and pulls node C high, thus turning on fourth switch 32n, which in turn pulls node D low, turning off third switch 30n. One of ordinary skill in the art would realize that when the first/fourth switches are open, the second/third switches would be closed, and vice versa. Thus, claims 7-10 are anticipated. Third/fourth switches 30n/32n are NMOS, and first/second switches 30p/32p are PMOS, anticipating claims 11 and 13. Related to this structure, one of ordinary skill in the art would know when switches 30p and 32n are conducting (allowing current to flow from Vdd to Vss through them and inductor 25), switches 32p and 30n are not conducting (e.g. zero current flow), and vice versa. Deeming each current within each respective transistor as a current they generate, claim 1 is anticipated. Gabara discloses a tank circuit, its relationship to capacitance (e.g. see column 2, lines 13-16), and operating at resonance/high efficiency (e.g. see column 2, lines 8-12). One of ordinary skill in the art would recognize the relationship between the capacitance, inductor 25, and the tank circuit, anticipating claim 2. Also, one of ordinary skill in the art would know resonant/high efficiency operation occurs when the input and output frequencies are the same, or at least substantially the same, thus anticipating claim 3.

This allows the maximum transfer of power. For example, if the frequencies are not close enough to one another, the circuit would provide an output signal with reduced gain, and a higher probability for having more noise. Interpreting Fig. 2A as showing first/second currents generated by NMOS devices 30n/32n, and the third/fourth currents generated by PMOS devices 30p/32p, claims 4 and 5 are anticipated. The currents generated will be geometrically proportional to the input signal, thus anticipating claim 6. For example, as the input signal to the gate of switch 30p decreases, its current will increase, the current through 32n will also increase, while the currents through 32p and 30n will decrease.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoover as applied to claim 7 described above. Although Hoover shows the basic structure of first-fourth switches and an inductor, the reference does not show/disclose the biasing as recited within claim 12, nor the integrated circuit as recited within claim 15. It would have been obvious to one of ordinary skill in the art to bias some or all of the transistors within Hoover's circuit near their cutoff region, rendering claim 12 obvious. With the transistors biased near their cutoff region, they would be able to switch on and/or off more quickly. Which transistors are to be biased would depend

upon what switching outcome is desired (e.g. faster high to low transition). It also would have been obvious to one of ordinary skill in the art to use the circuit of Hoover in an integrated circuit, rendering obvious claim 15. Most electronic circuits utilize integrated circuits, wherein the IC can provide compact size, decrease power consumption, and be easier to fabricate as a single unit/device instead of connecting a plurality of separate units/devices.

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara. It would have been obvious to one of ordinary skill in the art to reverse the transistor types/operations within Gabara's Fig. 2A circuit, wherein NMOS transistors 30n and 32n would be configured as the input pair of transistors receiving input signal Vpch, and PMOS transistors 30p and 32p would have their gates cross-coupled to the output nodes. In this configuration, the structure and operation of first-fourth switches 30p,32p,30n,32n and inductor 25 would render claims 7-11, and 13 obvious. The cross-coupled gates of PMOS transistors 30p,32p would provide a positive feedback, rendering claim 14 obvious. Using the same type of reasoning applied to the Hoover rejections described previously, claims 12 and 15 are rendered obvious. The near cutoff biasing would improve switching speed if that was desired, and an IC would be smaller, require less power, and be easier to fabricate.

Claims 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara as applied to claim 16 above. The circuit of Gabara reads on the basic limitations are described above. However, the reference does not show/disclose the fifth/sixth devices as recited within claim 17; the NMOS and PMOS devices as recited

within claim 18; or the integrated circuit, transceiver, and computing device as recited within claims 19-21, respectively. It would have been obvious to one of ordinary skill in the art to couple a fifth device between first device 30p and first output node C, and a sixth device between second device 32p and second output node D, rendering claim 17 obvious. For example, using a MOSFET for each fifth and sixth device, with its gate coupled to a bias voltage, the maximum amplitude of the output voltage could be controlled. The maximum amplitude would be increased when the first and sixth device are biased to provide a minimum of resistance, and when the resistance is increased by a corresponding change in the bias voltage, the upper level of the output signal's amplitude would be reduced. When the configuration of Gabara has its input and cross-coupled transistors reversed (i.e. 30p and 32p are cross-coupled, and 30n and 32n are used to receive the input signal), as related to the 103 rejections of claims 7-11 described previously, NMOS transistors 30n and 32n could be deemed the first and second device, while PMOS transistors 30p and 32p could be deemed the third and fourth devices, rendering obvious claim 18. Since Gabara discloses the use of MOS and CMOS technology for small size and low power consumption (e.g. see column 1, lines 9-14), it would have been obvious to one of ordinary skill in the art to form the modified circuit of Gabara on to an integrated circuit, thus rendering claim 19 obvious. Almost any circuit that uses an H-bridge type circuit could use the modified circuit of Gabara, including a transceiver or computing device with memory, central processing unit, and transceiver, thus rendering claims 20 and 21 obvious. Those uses are deemed intended use. The circuit of Gabara would provide a high-frequency, low-

power CMOS oscillator with a tunable tank circuit. The modified circuit of Gabara would merely change the amplifier from an input pair of PMOS transistors, to an input pair of NMOS transistors.

No claim is allowable.

The other prior art references cited on the accompanying PTO-892 are deemed relevant to the claimed invention. Although not used in any formal rejections described above, each of these references show and disclose known H-bridge type circuits with first-fourth switches/devices, and an inductor coupled between two output nodes. Therefore, each one would read on at least the limitations recited within at least independent claims 1 and 7. The references also show and/or disclose other limitations related to the claimed invention. Maggio et al. shows two of the switches/devices Q1,Q2 in Fig. 3 having their control electrodes cross-coupled with respect to the output nodes, thus providing a positive type feedback. Fig. 1 of Gersbach et al. shows an example of a capacitive/inductive type tank circuit 12 between the two output nodes. Linguet al. discloses an "elementary amplifying module" (e.g. see Fig. 2), and that the circuit can be related to a memory (e.g. see column 5, lines 39-40). Block 182 of Muri et al.'s Fig. 1 is related to a transceiver type system (e.g. see Fig. 3). Not only does Jusuf et al. show an inductor/capacitive tank type circuit in Fig. 3, but additional devices M3,M4 are coupled between first/second M1/M2 devices and their respective output nodes. Therefore, all of these references should be carefully reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

11 December 2001

Kenneth B. Wells
Primary Examiner